REMARKS

Reconsideration of the application, in view of the following remarks is respectfully requested.

The examiner rejects Claims 10 and 11 under 35 U.S.C. § 102(b) as being anticipated by Norris et al. The examiner has shown a picture of a shift register of the debouncing circuit of Norris and then stated, inter alia that the input of subsequent storage devices is selectivly coupled to the output to the previous storage device (the input of the subsequent flip-flop as selectively coupled to the output of the previous flip-flop).

This rejection is respectfully traversed. As it is clear from the figures that the examiner has produced in the offical action itself, the output of each of the flip-flops of the serial-parallel shift register are directly connected to the output of the previous stage. There is no circuit shown which can provide a selection of whether or not the input to one stage is coupled to the output of another, only a direct hardwired connection, which is not a selection. In view of the fact that '102 rejection must show all the elements of the claim, this rejection should be withdrawn.

The examiner rejectects Claims 13 and 16-20 under 35 U.S.C. § 103(a) as being unpatentable over Norris et al. The examiner states that the above noted CD 4015 shift register is a 4 bit shift register comprising 4 flip-flops that an 8-bit version is shown in the action. The examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an 8-bit shift register instead of a 4-bit shift register. However, Applicants did not understand the significance of the examiner's recitation of an 8-bit shift register instead of the 4-bit shift register, since none of the Claims 13 and 16-20 rejected by the examiner recite an 8-bit shift register.

Claim 13 is dependent upon Claim 10. The patentablility of Claim 10 having been shown

above, Claim 13 is patentable for the same reasons. Claims 16-20 are dependent directly or indirectly upon Claim 10. The patentability of Claim 10 having been shown above, Claims16-20 are patentable for the same reasons.

The examiner has not accepted Applicants selection of species and claims that read thereon. In so doing, he has withdrawn Claims 12 and 14 from further consideration. These claims are identical except for the claims upon which they depend, and both of those claims, Claims 10 and 13, are within the embodiment of Figure 5. Specifically, those claims recite the selection of the inputs to the flip-flops 512, 514 being selectively coupled to the output of the previous stage, 510 or 512, or the output of the memory device at line _st_se0_reg in Figure 5A. Therefore, clearly these claims should have been included within the claims considered by the examiner.

Furthermore, this points out the error in the examiner's reasoning that in Norris et al the outputs of the flip-flops are selectively coupled to the next stage, whereas the coupling is shown as a wire. In the present invention, specifically within Figure 5a, the selection means are the multiplexers 516 and 518, which is clearly not shown or suggested by Norris et al.

Accordingly, Applicants believe that the application including Claims 10-14, and 16-20 are in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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